III. REMARKS

Claims 1-20 are pending in this application. By this response, claims 1-6, 8, 12, and 16 have been amended. Applicants do not acquiesce in the correctness of the rejections and reserve the right to present specific arguments regarding any rejected claims not specifically addressed. Further, Applicants reserve the right to pursue the full scope of the subject matter of the original claims in a subsequent patent application that claims priority to the instant application. Reconsideration in view of the following remarks is respectfully requested.

In the Office Action, claims 1-6, 8, 12, and 16 are objected to based on various informalities listed in the Office Action. *See* Office Action p. 2. Applicants have amended claims 1-4, 6, 8 to comply with the Office's request. Applicants have also amended claims 5, 12, and 16 to partially comply with the Office's request. However, with respect to claims 5, 12, and 16, Applicants submit that the Office's suggestion regarding the addition of "the edge of the failing FET" is overly narrowing and unnecessary. Accordingly, no amendments with respect to that term have been made.

Claims 4-5, 11-12, and 16-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants appreciate the indication of allowable subject matter.

In the Office Action, claims 1-3, 6-10, 13-15, 19 and 20 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Applicants' admitted prior art, hereinafter "AAPA," in view of technical presentation view graphs entitled "BSIM4 Model and Parameter Extraction," prepared by Assenmacher, further in view of Alani et al. (US Pat. App. No. 2003/0182640),

hereinafter, "Alani." Reconsideration in view of the following remarks is respectfully requested.

With respect to claim 1, Applicants submit that the combination of references fail to teach or suggest each and every element of the claim, including "modifying an edge of a failing FET that is closer than a threshold distance to a well edge." (*See* claim 1, and as similarly recited in claims 8, and 15). The Office asserts that Assenmacher discloses that "...a FET having an edge that is closer than the threshold distance to a well edge should be modified (e.g., increasing the distance between a failing FET edge a nearby well edge)." *See* Office Action, p. 5. In response, Applicants submit that Assenmacher is merely an example of well proximity modeling, which alone does not disclose or suggest the actual step of modifying an edge of a failing FET. Simply because a distance to a well edge *should* or *could* be modified, as asserted by the Office, does not provide a teaching of doing so. Alani also fails to disclose modifying an edge. Accordingly, Applicants submit that the combination fails to teach or suggest every element of the claimed invention.

With further respect to claim 1, Applicants submit that none of the cited reference teach or suggest each and every element of the claim, including, "identifying any field effect transistor (FET) that causes a signal integrity failure in the case that the IC design fails the signal integrity analysis." (*See* claim 1, and as similarly recited in claims 8, and 15). As admitted by the Office, AAPA fails to disclose, *inter alia*, "...a method of identifying any FET in an IC design that may cause a signal integrity failure." Office Action, p. 3. However, the Office asserts that Assenmacher "teaches a method of using parameterized SPICE well proximity macro (FET) models using distances of devices (i.e., FET's) to well edges as instance parameters in evaluation of threshold voltage Vt degradation of devices (FET's) in an IC design..." (Office Action p. 3-4).

Applicants submit, however, that Assenmacher fails to disclose identifying any field effect FET that causes a *signal integrity failure*. (Emphasis added). The claimed invention teaches a signal integrity failure in the case that the IC design fails the signal integrity analysis (*see* claim 1), while Assenmacher merely discloses a threshold voltage increase during NWell proximity effect modeling. Assenmacher at 18. Likewise, Alani simply discloses a signal integrity analyzer, but does not disclose or suggest identifying any failing FET. Accordingly, Applicants submit that the combination of references fail to identify any FET that causes a signal integrity failure during signal integrity analysis on an IC design.

With regard to the rejection as a whole, Applicants respectfully submit that the Office's logic in combining the references is very weak. The Office's asserts: AAPA discloses signal integrity analysis and that well proximity affects threshold voltage, and Assenmacher discloses well proximity analysis to evaluate threshold voltage. The Office also asserts that Alani discloses signal integrity analysis and it discloses a well proximity macro. With regard to this latter assertion, Applicants submit that mere disclosure of 3rd party SPICE tools generally, fails to provide disclosure of SPICE well proximity macro models, as asserted by the Office. Alani simply recites that "[t]he third party tools 110 may include, for example, sub-circuits from other tools, such three-dimension (3D) extraction tools." ¶ 0025. However, Alani provides no disclosure of any SPICE well proximity macro models, as asserted by the Office.

Based on the alleged disclosures outlined above, the Office combines the references to render the claims obvious. Applicants assert, however, that there are a number of flaws in the Office's logic. In particular, the Office is modifying AAPA with Assenmacher to teach well proximity analysis, and then is modifying Assenmacher with Alani to teach signal integrity

analysis of a circuit layout. That is, the fact that the Office has modified the secondary reference (Assenmacher) with the third reference (Alani) and combined the result with AAPA to support the alleged obviousness rejection, makes the suggestion/motivation argument immediately suspect. More specifically, there is simply no suggestion or motivation, excepting Applicant's disclosure, for using modifications of a well edge to correct a signal integrity failure. The fact that Assenmacher evaluates well proximity for threshold voltage analysis does not mean that it is logical to extend well proximity analysis (and modification) to address signal integrity failures. The references simply do not support this conclusion, especially since, contrary to the Office's assertion, Alani does not disclose well proximity analysis simply by the mentioning of a SPICE file. Accordingly, Applicants request withdrawal of the rejection.

With respect to dependent claims 2-7, 9-14, 16-20, Applicants herein incorporate the arguments presented above with respect to the independent claims from which the claims depend. The dependent claims are believed to be allowable based on the above arguments, as well as for their own additional features.

IV. CONCLUSION

In light of the above, Applicants respectfully submit that all claims are in condition for allowance. Should the Examiner require anything further to place the application in better condition for allowance, the Examiner is invited to contact Applicants' undersigned representative at the number listed below.

Respectfully submitted,

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